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Low Power and High Speed 6T SRAM Cell in Nanoscale CMOS Technologies

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Abstract

With the development of CMOS technology in progress beyond 100 nm, It has become more and more difficult to deal with power. The performance targets for different product applications have been subjected to the aggressive gradient in the development of static access memory (SRAM). In this paper, a new design of the low power SRAM cell is used for high speed operations. The model uses the voltage mode used to reduce voltage fluctuations when changing the writing activity. Dynamic dispersion increases with the frequency of SRAM cell function. In this proposed design, we use voltage sources connected with BL (Bit) and BAL (Line Line) lines to reduce voltage fluctuation during the write operation "1" or write "0". The simulation using LT Spice IV is performed in 90 nm CMOS technology with a voltage of 1V. The dynamic capacity is calculated for different frequencies such as 500 MHz, 1 GHz and 2 GHz. We compare it to the traditional SRAM 6-T cell. The results of the simulation show that the power loss is almost constant even at the highest frequency of the proposed SRAM model. This justifies the reduced power consumption of RF CMOS VLSI radio frequency design.

Keywords: CMOS, RAM, ROM, BL, WL, SRA, BLB, VTC**.**

Introduction

Today, chip regulation is still a fast-moving market. It has provided increasingly complex functions that require increased memory capacity. Random Access Memory (SRAM) is the most commonly used solution, where bandwidth or low power, or both, are key considerations. Unlike the DRAM (dynamic random access memory), the SRAM uses a memory chip, so the periodic update is not necessary and the static word indicates that there is close two locks to save each bit. Semiconductor memory. SRAM displays the remaining data, but remains volatile in the sense that the data is lost when the memory does not work. It is also easier to control the SRAM (interface to) and to access more deeply the actual types of DRAM.

The increased demand for larger storage capacities for data and memory development of manufacturing technology has led to more compact design rules, increasing the density of data storage. The memory arrays on the slide are now widely used in many VLSI circuits. The effectiveness of the memory area, ie. The number of data bits stored per unit of space is one of the key design criteria that determines the total storage capacity and therefore the memory cost per bit.

With the development of integrated memory technology, DRAM and SRAM are prevalent in today's chip system. Exchanges between big and small memories of all sizes made things easier, allowing Sunni companies to focus more than ever on systems at the board level. The large SoC integrated memories offer a number of advantages, such as improved bandwidth and high performance, which can only be achieved by using integrated technologies. The ability and success of incorporating large DRAM and / or SRAM blocks into the SOC depends primarily on the manufacturing capacity.

The SRAM cell contains three different states that can be activated: sleep mode when the circuit is idle, reads the time to request and write data when the content is updated. The SRAM must operate in read mode, read-write stability, direct write capability. It is difficult to meet both conditions in advanced techniques because of the high degree of contrast in the parameter of the thin CMOS transistor, mainly technologies exceeding 45 nm. Increasing the amount of memory makes the reliability required difficult. This is the first challenge for SRAMs in advanced technology nodes. The high power consumption of portable electronic devices is a matter of serious concern. Reduced battery life, additional packaging and cooling requirements are associated with high energy consumption. Constant power dissipation due to leakage currents is an important component of total energy dissipation. Electronic devices contain different types, including many inactive components that account for a large part of the total energy dissipation of the system.

Growing demand for portable battery operating systems makes high-efficiency processors, for the applications such as the efficiency of portable computing, the top priority. These compact systems require frequent recharging of their batteries. The problem is more serious in wireless sensor networks deployed to monitor environmental standards. These systems may not be able to charge the batteries. We know that chip memories determine the dissolution of SoC chips. It is therefore very important that you have energy-efficient, low-power SRAM memory and that you use it primarily in smart memory. Many methods are adopted to reduce energy dissipation, such as gradient voltage difference circuit design, feeding methods, and drowsiness. A low supply voltage reduces the dynamic energy squared and leaks exponentially. But expanding the supply voltage reduces the noise margins. Many SRAM matrices depend on the reduction of the active capacitance and the oscillation voltage.

Integrated SRAMs provide a direct means of bringing the advantages of a densimeter to circuit and architecture level transistors. They are therefore vital for this new model of measuring integrated circuits. Because of its consistent structure and applicability to many digital systems, SRAM has been carefully designed as a key component in the development of new technology nodes and uses highly specialized and bold planning rules that take into account secondary manufacturing constraints. This level of attention paid to the design of the SRAM bit cells made it possible to follow the evolution of the density according to the same transistors.

Design technique of SRAM CELL

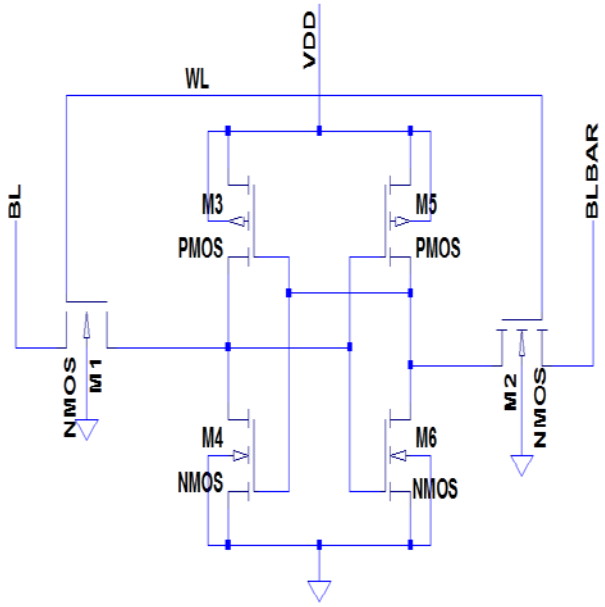

Figure 1 : Basic Circuit Diagram of SRAM Cell

Figure 1 shows the actual SRAM architecture built on CMOS adapters. It consists of two inverted back-to-back couplers A and B, two transistors to reach M1 and M2. An access transistor is connected between the inverter and the BL and BLB bit lines, and their gates are connected to WL. The access transistor allows writing and reading across the word line and can be stopped while stopped. The port itself is used for reading and writing. In order to ensure that the cell operates, it is necessary to properly design the transistor.

The SRAM cell can store data bits. The SRAM comprises two connected duplexers and two access transistors. The access transistor is used for writing and reading access to the cell. The SRAM cell provides the following basic properties.

- Retention: An SRAM cell can retain the data indefinitely while it is activated.
- Read: SRAM cells can connect data. This process does not affect the data. In other words, the reading process is not destructive
- Write: SRAM data can be defined for any binary value, regardless of its original data.

Many topologies of SRAM cells have been reported over the past decade. Among these topologies, the four-transistor cell received a 4T weighing cell, an unloaded 4T cell and an SRAM cell of six (6T) transistors have aroused interest because of their coherence when storing the logic. a "and" zero ". "[4] The data retention in the SRT 4T cells is provided by the leakage current of the transistors, so it is not suitable for low power applications, but the data stability in the SRAM 6T is independent of the current. The 6T configuration offers a much greater noise tolerance, a particularly important feature of noise reduction techniques, the main reason for the popularity of SRAM 6T in low-power SRAMs instead of 4T configurations. It consists of two CMOS and two access transistors. Build the output (input) of the inverter's internal node. The access transistors facilitate the connection of the internal nodes of the cell to the I / O ports of the inverter. cell,

called input / output ports of the cell with BL and BLB (bit lines) Bit lines are a way of communicating data between cells in the same column of a cell network. And so have a high capacitive load. The read and write operations are performed by bit lines as we will see in the following sections.

Proposed SRAM CELL

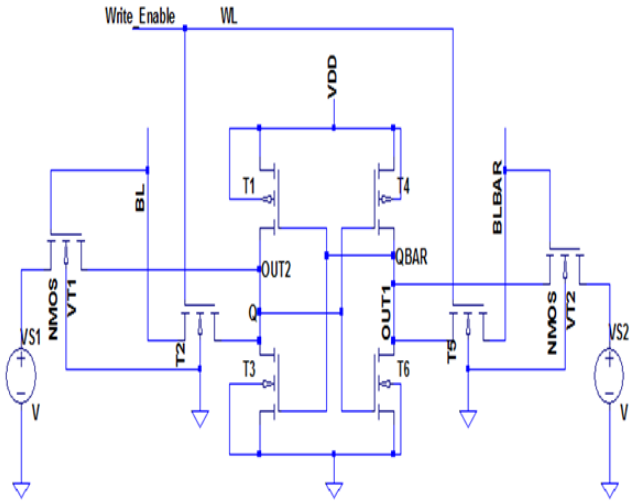

Figure 2 : Proposed SRAM Cell

The proposed SRAM cell schema is designed and implemented using LT SPICE IV. For simulations, we use a 1V power supply for different frequencies. VS1 and VS2 were taken with 0.5 volts during the simulation. These simulation results are compared to the traditional SRAM 6T cell.

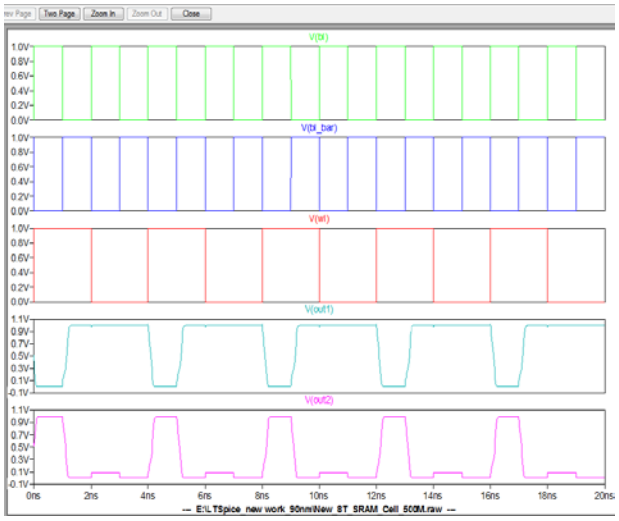

Figure 3 : Proposed SRAM cell for 500 MHz

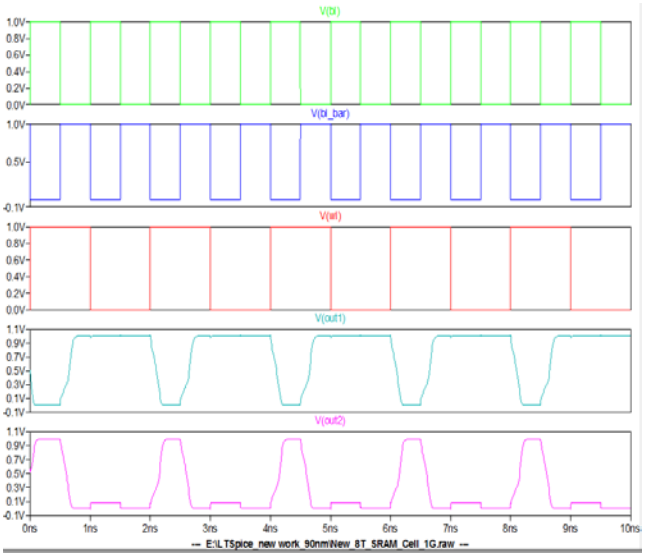

Figure 4 : Proposed SRAM Cell for 1 GHz

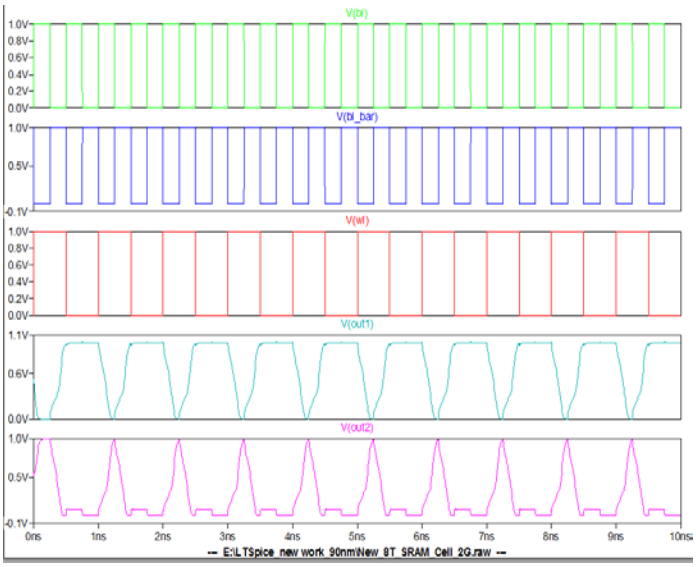

Figure 5 : Proposed SRAM Cell for 2 GHz

We simulate the proposed SRAM cell for 500 MHz, 1 GH and 2 GHz respectively. The simulation results for 500 MHz and 1 GHz, respectively, were presented in 3 and 4 respectively. Images 3 to 4 clearly show that the loading and loading of bit lines and small channels have been improved for high operating frequencies.

In the end, we calculated the energy crisis in the proposed 500 MHz, 1 GHz and 2 GHz SRAM compared to these results compared to the traditional 6 chamber SRAM cell comparison. Table 1 shows the width and length used in the proposed model. The proposed model was simulated in 90 nm CMOS technology. We therefore chose 90 nm more for all transistors. The comparison between the average electric MRS current and the model proposed in Table 2 is indicated.

It is aware that if the traditional SRAM cell is multiplied by the operating frequency, the energy dissipation is almost double, but that in the case of the proposed SRAM power, the low energy at different frequencies is almost half almost

constant by compared to traditional SRAM. Cellular Therefore, it is clear from the findings that the proposed approach for CMOS-based SRAM design is suitable for high speed VLSI designs.

TABLE 1 : Width and length used in the proposed model for Simulation

Transistors	Widths(nm)
T1	175
T2	115
T3	500
T4	175
T5	115
T6	500
VT1	300
VT2	300

TABLE 2 : Comparison of Power Dissipation between the New Design Cell Vs Conventional SRAM Cell

Operating frequency	Power Dissipation in 6T SRAM cell (µW)	Power Dissipation in Proposed SRAM cell (nW)
500MHz	4.890	606.519
1GHz	8.002	606.519
2GHz	11.979	606.519

In the proposed SRAM cell, the single line, WL and output voltage values are increased compared to the traditional SRAM cell, but these values can be controlled by the size of the width (W) and the length (L) of the transistor.

Conclusion

There are two main types of power consumption, and there is a major problem in the high-speed VLSI design that drives mobility. In this article, we present a new design for low power dynamic SRAM cells that use voltage mode. The proposed SRAM has two voltage sources to reduce the fluctuations of the output voltage during the conversion voltage. Voltage fluctuations reduce the dynamic energy dispersion. The proposed dynamic update of the new SRAM cell is almost constant for high-speed operation. Due to the large number of transistors and regions compared to traditional SRAM 6AM cameras, this defect can easily be eliminated with very low power consumption at a very high frequency. The proposed SRAM memory can be used to provide low-power solutions, such as laptops, smart phones, and programmable logic devices for high-speed devices.

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