ijergs
Open Access
International Journal of Engineering Research and Generic Science (IJERGS)
Available Online at www.ijergs.in
ISSN: 2455 - 1597
Volume -3, Issue - 4, July - August 2017, Page No. 07 - 11

Amelioration of Seven Level Inverter by Using POD and PWM Methods

Ch.Shireesha[1], Dr.Jaghannath.K[2], D.Kumara Swamy[3]

[1]M. Tech scholar, Dept of EEE, SVS Institute of Technology, Hanamkonda, T.S, India

[2]Assistant Professor, Dept of EEE, SVS Institute of Technology, Hanamkonda, T.S, India

[3]Associate Professor, HOD, Dept of EEE, SVS Institute of Technology, Hanamkonda, T.S, India

Abstract

After all the multilevel inverters carry be victorious features, formula of added switches in the common place arrangement bearing a disadvantage to its roomy distance employment .There is a development of pod techqunic with 7 level inverter using the dc link and it is capable of generating 7 levels output with less component count it uses single carrier wave and two sine waves for pulse generation the total project is executed in the Matlab/simlink. There is an analysis of connecting R–load

Keywords- Switch Topology, Mos-fet, Micro Controller; Multilevel-Inverter; POD Technique, Pulse Width Modulation (PWM).

1. Introduction

Inverter is converting uncontrolled D.C. in to control A.C. There are so many types of inverter like two levels, three level and five level etc. In this paper seven level inverter has discussed and it' results. Seven level inverter has made up of D.C. source, 12 power electronic devices (ideal switches), star connected resistive load, and (with 180 deg.conduction mode) .Sinusoidal Pulse Width Modulation (SPWM) technique is used to generate the gate pulses. SPWM technique is widely used in industries. Cascaded seven Level Inverter is discussed in this paper. FFT is used for harmonic analysis of output of Seven Level Inverter. The paper is organized as follows: Section 2 explains the cascaded H- bridges. Section 3 discusses the sinusoidal pulse width modulation technique. Section 4 explains the circuit description of seven level converters. Test cases and simulation results for single and seven levels are given and discussed in Section 5, 6. In section 7 discusses comparison of power component requirements per phase leg among three multilevel inverters and conclusions in Section 8

2. Cascaded H-Bridges

A single-phase structure of an m-level cascaded inverter is illustrated in Figure1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or Hbridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc , 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches, S 1 , S 2 , S 3 , and S 4 . To obtain +Vdc , switches S 1 and S 4 are turned on, whereas –Vdc can be obtained by turning on switches S 2 and S 3 . By turning on S 1 and S 2 or S 3 and S 4 , the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources [5].

3. Sinusoidal Pulse Width Modulation Technique

This is a very simple technique for harmonic reduction. In this technique pulse magnitude will be constant and only pulse time (width) can be changed. In this pure sine wave is compared with carrier (triangular) wave and producing gate pulses. Sine wave has fundamental frequency and carrier wave can be taken more than fundamental frequency. Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. In the modulation techniques, there are two important defined parameters: 1) the ratio P = ωc/ωm known as frequency ratio, 2) the ratio Ma = Am/Ac known as modulation index, where ωc is the reference frequency, ωm is the carrier frequency, Am is reference signal amplitude and AC is carrier signal amplitude.

4. Sampling Technique

In this method of modulation, several pulses per half-cycle are used. Instead of maintaining the width of all pulses, the width of each pulse is varied proportional to the amplitude of a sin-wave evaluated at the centre of the same pulse. By comparing a sinusoidal reference signal with a triangular carrier wave, the gating signals are generated. The frequency of reference signal determine the inverter output frequency and its peak amplitude, controls the modulation index, M, and then in turn the RMS output voltage in Fig3 shows the more common carrier technique, the conventional sinusoidal pulse width Modulation (SPWM) technique, which is based on the principle of comparing a triangular carrier signal with a sinusoidal reference waveform (natural sampling).The figure below gives the sinusoidal pulse width modulation.

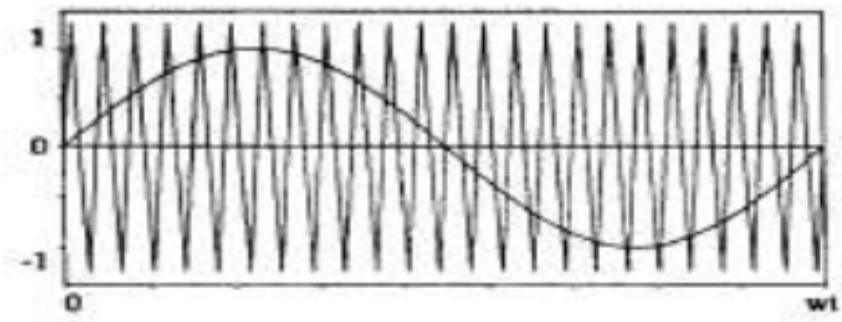

Figure: Carrier Alignment of POD PWM

Proposed Cascaded Multilevel Inverter

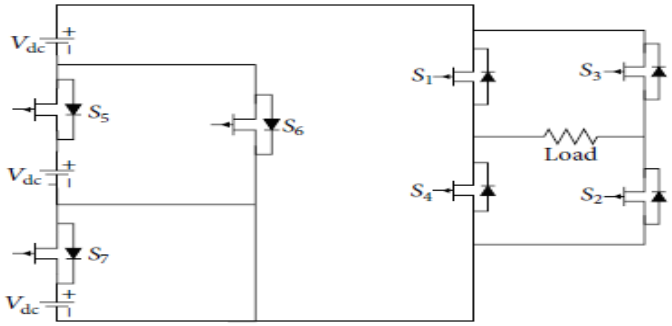

Figure: 7-Level 7-switch topology

Table: Switching Scheme for Seven Level Seven Switch Topology

SL no.	S_4	S_5	S_6	S_7	S_1	S_2	S_3	Output voltage
1	ON	ON	ON	OFF	OFF	OFF	ON	+Vdc
2	ON	ON	OFF	OFF	OFF	ON	OFF	+2Vdc
3	ON	ON	OFF	OFF	ON	OFF	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	ON	ON	OFF	−Vdc
6	OFF	OFF	ON	ON	ON	OFF	ON	−2Vdc
7	OFF	OFF	ON	ON	OFF	ON	ON	−3Vdc

Aiming at reducing the switches to the maximum possible extent and reducing complexity, the new topology is introduced with 7 switches for 7 levels, and this would be the least possible reduction. The new MLI configuration is made of 7 switches 7-level topology in a special arrangement with3 inputs DC sources to generate 7 level output. The less switches we use lessen the cost of circuit building. The circuit credibility is checked without using pwm. Then identifying the effectiveness in working simulated the circuit with PD, POD, and APOD using MATLAB/SIMULINK.

(1) **Conventional Topology.** Using 3 DC voltage sources, 3H-bridge units each with 4 switches together forming 12switches in total are used in conventional CMLI which is represented in Figure 1.General expression for output voltage levels, $m = (n + 2)/2$ where n is the number of switches in the configuration. Each Bridge is outputting 3 Levels, $+V$dc,0, $-V$dc. Cascading 3 Bridges in such a fashion to produce stepped 7 level staircase waveforms.

(2) **Existing Topology**

(a) ***7-Level, 9 Switches***. This topology is built with 3 dc sources, 1 H-bridge composed of 4 switches and then additional 5 more

Switches for producing stepped 7 levels, for positive and negative half cycles. Table 1 represents the switching scheme for this topology.

(b) *7-Level, 7 Switches.* This topology is made of 7 switches and 3 dc sources and is shown in Figure. One Hbridgepresent in the topology is mainly for polarity change. Here, three switches conduct at a time for level generation.

(c) ***7-Level, 6 Switches***. This is a special configuration consisting of four dc sources and six switches. One switch across the load is used for zero level. *S*1, *S*2, *S3* used for level generation and *S*4, *S*5 switches for polarity changing Figure 4 represent the 7-level6-switch topology and the corresponding switching pattern

5. Simulate Non Analysis and Results

Simulation of proposed multi level inverter is carried out in MATLAB/Simulink .ln Figure 4 Dc supply of 100 volts is given using batteries and 2 dc link capacitors are used and 8MOSFET are used as switches and output of multi level Inverter is connected to L,C filter to eliminate harmonics. The technique used for pulse generation is POD technique. Generally in order to turn on 8 switches 8 carrier signals are needed but using proposed technique single carrier wave is used to generate switching pulses to 8 switches. Voltage measurement device is connected across each capacitor to measure the voltage across the capacitor

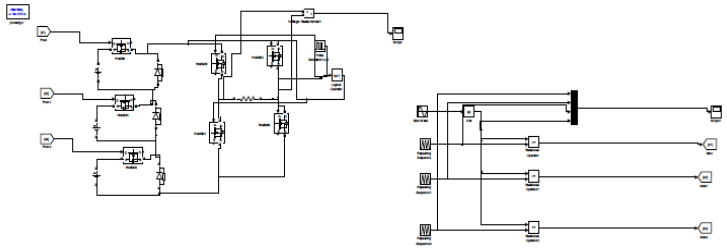

Figure: Simulink model for single level inverter

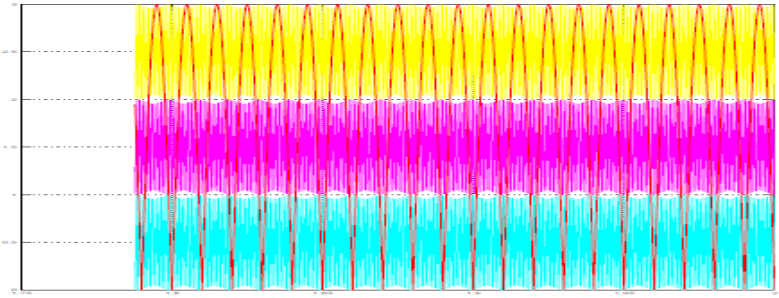

Figure: Output voltage waveform

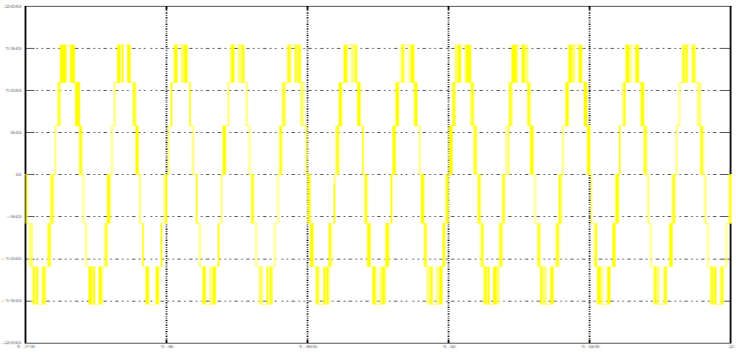

Figure: Seven level output of proposed topology

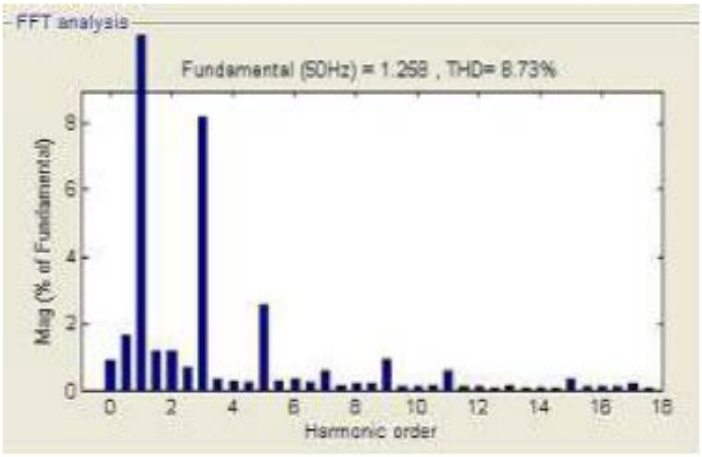

Figure: 6 FFT analysis of seven level inverter

References

[1]. M.Li, J.N.Chiasson, L.M.Tolbert, "Capacitor voltage control in a Cascaded Multilevel Inverter as a Static VArGenerator," *IEEE* 5th *International conference on Powerelectronics and motion control*, Vol. 3. 2006

[2]. Fang Zheng Peng, Jih-Sheng Lai,"Dynamicperformance and control of a Static Var Generator Using Cascaded Multilevel Inverter," *IEEE Transactions on Industry Applications*, Vol. 33, No. 3,May/June 1997.

[3]. Fang Zheng Peng, Jih-Sheng Lai,"A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation," *IEEE Tran*sactions on *Industry Applications*, Vol. 32, No. 5.September 1996.

[4]. T.Manokaran, B.Sakthivel, S.Mohamed Yousuf,"Cascaded Multilevel Inverter Based Harmonic ReductionIn Statcom," *International Journal of Engineering Scienceand Technology*. Vol. 2(10), 2010.

[5]. Jagdish Kumar, Biswarup Das, PramodAgarwal,"Modelling of 11-Level Cascaded MultilevelStatcom," *International Journal of Recent Trends in Engineering*, Vol 2, No. 5, November 2009.

[6]. G.Sundar, S.Ramareddy, "Digital Simulation of Multilevel Inverter Based Statcom," *Journal of Theoreticaland Information Technology*.JATIT 2005