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Improve performance of Adder/Subtraction

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Abstract

The Reversible logic gate is evolving to be difficult for future computing innovations. It is progressing as the fundamental field of research that concern general uses in the domain such as CMOS design (reduced power). In this work, the recommended summary of complete adder/subtractor circuit using Reversible logic gates (Fault Tolerant). We recommended a complete adder/subtractor by employing COG (Controlled Operation Gate) and MIG (Modified Islam Gate) Reversible logic gate with the intelligence. One can easily deduce form the Results section that a setback can be reduced as much as 61% when utilizing COG and MIG Reversible logic gate compared to the complete adder/subtractor founded on the FDG (Feynman Double Gate).

Keywords: *COG, MIG, Complete Adder, Set-back, Reversible Gate, Fredkin Gate, Feynman Double Gate.*

1. Introduction

Quantum computation is now on the forefront of hypothetical and practical research. The study into the changeability and Reversible conduit is acknowledged to be more prevalent as changeability is the pre-requisite of a quantum computation. Arbitrarily, the restrictive characteristic of changeability compels a construction on conduits, for instance, a microprocessor engineering is significantly more acceptable for investigation, within the framework of Reversible conduit plan as well as for common conduit intricacy. The Reversible conduits [1,2 and 3] and Reversible computation [4. 5] constrain every gate and every calculation step to be fully Reversible such that there is no loss of information at any advancement of the algorithm. It does not participate in the dissemination of heat in the conduits. Hence, they possibly try to solve at least two problems, namely energy sparing and overheating and this implies lengthier lifespan for the batteries. The Reversible logic organization could be especially fundamental in low-voltage portable system types, where overheating and energy sparing both are necessities given the need for autonomous and insubstantial energy source. The calculation gadgets, for instance processors, can be devised to not need the power dispersal [4, 6], though on the condition that the computation is logically Reversible. The strategy is a complete exit from traditional reduced power and logic plan methods. For practically Reversible calculation which do not disseminate energy at all, the electronic device has to be consistently reversible and engineered in the practically reversible technology [7]. A body that changes state from A to B will be said to be practically reversible if the state B particularly determines state A, implying that the transformation was logically reversible, and energy is available to undergo the reverse transformation, signifying that the transformation was executed in a practically reversible technology. Reversibility inexorably compels architectural needs that are not satisfied by conventional processors.

Traditional computing devices execute the irreversible calculations. Such calculations ruin the data, while the 2nd law of Thermodynamics requires a basic dissemination of energy when the data bit is removed. The decimal mathematics field is getting consequent notice as an online, business and financial-founded applications and may not accept the faults created by the change involving binary and decimal types [8].

2. Basic Reversible Logic Gates

A. Feynman Gate

The Feynman Gate (FG) is one 2*2, all over the reversible gate as shown in the figure 1. The input vector is I(A,B) while the output vector is O(P,Q). The outputs are defined by P=A, Q=A.B. The Quantum Cost, QC of the Feynman gate is 1. The FG is used as a duplicating gate. As diffusion is not authorized in reversible logic, this gate is useful for copying of the necessary outputs.

The Fredkin Gate like CSWAP gate is a calculation circuit suitable for the reversible calculations, and it was introduced by Ed Fredkin. It is complete, this suggests that any mathematical and logical process may be evolved along with the Fredkin gates. The Fredkin gate is one 3-bit gate that exchanges the preceding 2 bits if the major bit is 1.

The basic Fredkin gate is an organized exchange gate that superimposes the three inputs, namely C, I1 and I2 on top of the three outputs namely C, O1, O2. The input 'C' is particularly superimposed on the output 'C'. In case C=0, then no exchange is executed; I2 is superimposed on O2 and I1 is superimposed on O1. Another feature is that the two outputs are exchanged such that I2 is superimposed on O1 while I1 is superimposed on O2. It is simple to deduce that some circuits are reversible, meaning that it "undoes" itself when executed in reverse. The n×n Fredkin gate goes by its initial n-2 inputs unchanged to its analogous output.

The Fredkin gate is one reversible three bit gate that exchanges its preceding 2 bits if original bit is 1.

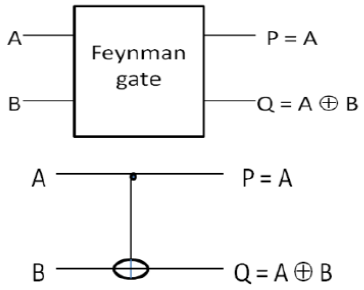


Figure 1: Feynman Gate

B. Toffoli gate

The Toffoli gate (further CCNOT gate) of the logic conduits was introduced by Tommaso Toffoli. It is a common reversible logic gate, meaning that the Toffoli gates can be used to construct any reversible conduit. This gate is also known as "controlled- controlled- not" gate and this represents its task. It has three bit inputs and outputs; if the first two bits are fixed, it converts the third bit; otherwise, all the bits keep functioning till completion. The logic gate L will be reversible in the case that there is an input x for every output y, to a point of executing L(x)=y. If gate L is reversible, then there is an opposite gate L′ that superimposes y onto –x for which L′(y)= x. NOT is reversible from standard logic gates as may be perceived from the truth table below.

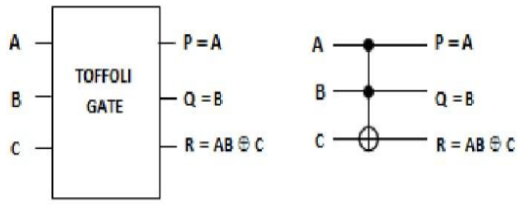


Figure 2 :Toffoli Gate

The essential AND Gate is not reversible, though. All of the inputs 00, 01 and the 10 are superimposed onto an output of 0. Researchers have focused on the Reversible gates as early as the 1960s. The original motivation was the reversible gates that could diffuse the minimum of heat (or, ideally no heat). In a simple gate, the input conditions are destroyed as fewer information is accessible in the output compared to what was accessible at input. This destruction of information wastes the energy to the surrounding area as heat, because of thermodynamic entropy. An alternative method to understand this is the charges in the conduit which are Earthed, but which flow away afterwards by keeping a small quantity of energy with them when altering their state. A reversible gate simply shifts the states around; as information is not destroyed, energy is restrained. The latest incentive comes from quantum calculations. Quantum mechanics necessitates the conversion to be reversible, though it allows for more extensive settings of the computation (superpositions). Thus the reversible gates organize a division of gates that are authorized by quantum mechanics, and in case we devise anything reversibly, we may treat it using a quantum-computer.According to the compartment principle, a reversible gate should have similar input and output bits. For one input bit, there have to be two possible reversible gates, one of which is NOT while the second one is the character gate which superimposes its input onto its output without modifications. Of the two input bits, the essential consequent gate is an organized NOT- gate that can XOR its initial bit to the second bit, while leaving the original bit unaltered. Regrettably, there are reversible processes cannot be treated by employing only such gates. Thus, the series constituting of NOT and XOR gates is not whole. In case we have to estimate a random process by utilizing the reversible gates, we necessitate a different gate. One likelihood will be a Toffoli gate as the Toffoli proposed in 1980.

C. Double Feynman Gate (F2G)

Figure 1.3 illustrates the 3*3 Double Feynman Gate. The I (A, B, C) is the input vector and O (P, Q, R) is the output vector. The outputs are defined by P= A, Q= A B, R= AC. The quantum price of the Double Feynman Gate is 2.

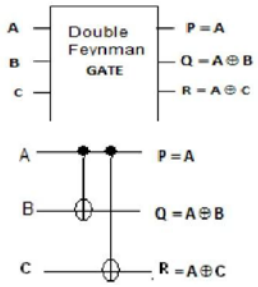


Figure 3: Double Feynman Gate

D Fredkin Gate

Figure 1.4 depicts the 3*3 Fredkin gate. I (A, B, C) is the input vector while O (P, Q, R) is the output vector. The output is defined by P= A, Q= A′B AC and R= A′C AB. The quantum price of the Fredkin Gate is 5.

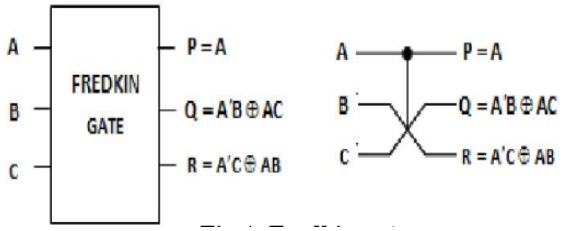


Figure 4: Fredkin Gate

E. Peres Gate

For the Peres Gate, I (A, B, C) is the input vector while O (P, Q, R) is the output vector. The output is defined by P= A, Q= AB and R= ABC. The QC of the Peres Gate is 4. In the proposed plan the Peres gate is employed on a number of its minimum quantum cost.

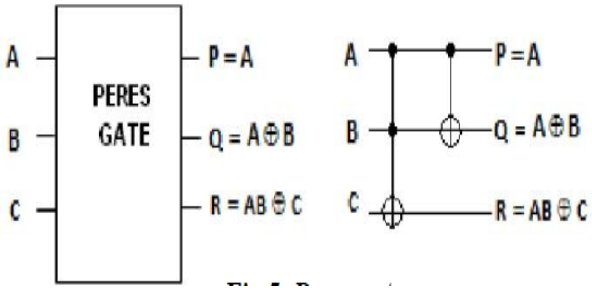


Figure 5: Peres Gate

The complete-adder by using the two Peres gates is shown in Fig 1.6. The Quantum recognition specifically illustrates its QC is 8 where two Peres Gates are employed. A solitary 4*4 reversible gate is termed the PFAG gate where QC of 8 is utilized to comprehend the multiplier.

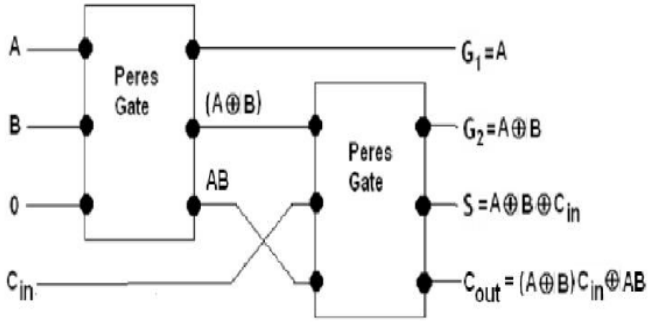


Figure 6: Full Adder By Peres Gate

F. TSG gate

For the TSG gate, I (A, B, C, D) is the input gate and O (P, Q, R, S) is the output gate. The output is defined by P= A, Q= A'C' xor B', R= (A'C' xor B')xor D and S= (A'C' xor B').D xor (AB xor C). The QC of the Peres gate is 4. The Peres gate is used based on its minimum QC. It may be verified that the input plan is connecting to a particular output plan may be astoundingly determined. The proposed TSG gate is ready for performing each Boolean function and may similarly operate autonomously as a reversible complete adder.

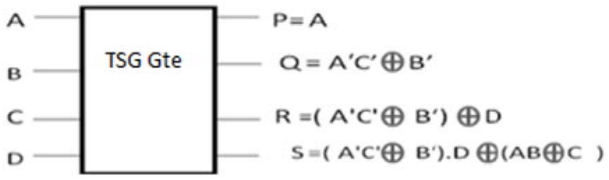
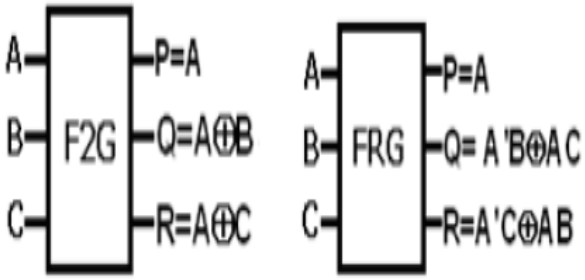


Figure 7: TSG Gate

3. Parity Preserving Reversible Gates

The error leniency is the characteristic that enables the structure to work easily and to maintain an adequate functioning in the event of a failure in some portions. If the structure itself created the error leniency components, then the sensing and rectification of the errors will turn out to be less challenging, uncomplicated and easier. Similar to a multitude of diverse frameworks, adjustment, the error leniency is achieved by the equivalence. As such, the equality sparing reversible conduits is going to be the future proposal pattern to a progression of error lenient reversible structures in nanotechnology. Additionally, the gating system is said to be equality sparing if every one of its gates are equality safeguarding [5]. A few equality sparing logic gates have been recommended in the literature, for example the 3*3 F2G shown in Figure 3.2(a) and 3*3 FRG shown in Figure 3.2(b) that are one-through gates, meaning that one of the contributions is also the result.

It can be deduced from Tables 3.1 and 3.2 that the gates F2G and FRG are individually equivalence conserving as they satisfy the requirement of A XOR B XOR C= P XOR Q XOR R. Moreover, for any k*k reversible logic gate to be equivalence preserving, the contribution EX-OR has to harmonize with an EXOR of results.



(a) **(b)**

Figure : 7: (a) F2G (Feynman Double Gate), (b) FRG (Fredkin Gate)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

TABLE No.1: Table of the Parity Preserving F2G (Feynman Double Gate)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

TABLE No. 2. Table of the Parity Preserving FRG (Fredkin Gate)

The enforcement of reversible logic utility of the adder conduit has been considered by some authors in literature reviews. The [12] demonstrates that the reversible adder conduit can be recognized with a minimum of 2 waste results and one steady contribution. The requirements of the error lenient reversible adder conduit are not similar because here the input equivalence has to be the same as the output equivalence. The specific portion initially details the mid adder/subtractor unit by using various circuits as intended. It is achieved by assuming to have the minimum quantity of waste output and the required steady inputs. This paper suggests one more error lenient, complete adder/subtractor conduit that was inspired by the sequential binary adder/subtractor conduit.

A. Design of Half Adder/Subtractor Circuit (FTHA_S)

For planning such a structure, the fundamental equivalence preserving reversible gates that are used are the F2G and the FRG as characterized in a previous section. The regular Boolean expression for a half adder is:

$$Sum = A \text{ XOR } B \qquad \ldots\ldots (3.1)$$

$$Carry = A \text{ and } B \qquad \ldots\ldots (3.2)$$

The Boolean expression for a half subtractor is:

$$Difference = A \; XOR \; B \qquad \ldots\ldots (3.3)$$

$$Borrow = \bar{A} B \qquad \ldots\ldots (3.4)$$

It can be deduced from the above equations that the conditions (3.1) and (3.3) are similar. The major differences are in the expressions for carry and borrow. The direction of any limit line is proposed in this specific field for implementing the conduit that may function as the adder as well as the subtractor. Figure 3.1 shows the attention that the suggested plan was using the F2G and the FRG that are both reversible and characteristically equivalence preserving. There are two contributions An and B as well as the limit line 'ctrl' that controls the technique of the process. The moment 'ctrl' is at the logic 0, then the conduit functions as the half adder and if 'ctrl' is at the logic 1, the conduit executes a subtraction. The summation and diversion line is represented as the S/D and the corresponding carry and borrow by C/B. The remaining four contributions that are called the constants are forced to the logic 0 and the waste signals are g1 to g5. It is displayed in Figure 4 that the FTHA_S (fault tolerant half adder/subtractor) conduit compels seven contributions and the matching seven results, as per the reversible rule. The proposed conduit may execute the summation and subtraction by employing a solitary circuit, though this is not beneficial in terms of energy sparing, instead it is useful for the cost. The Boolean expression suggest the conduit to be as follows:

$$S/D = A \; XOR \; B \qquad \ldots\ldots (3.5)$$

$$C/B = \overline{Ctrl}\, AB + Ctrl\, \bar{A} B \qquad \ldots\ldots (3.6)$$

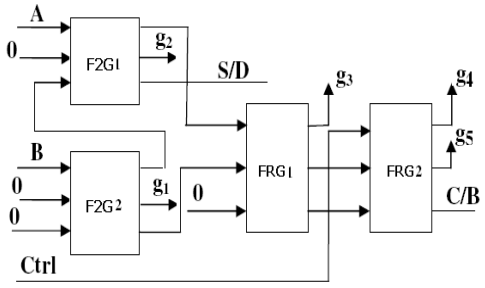


Figure 8: The Reversible Fault Tolerant Half Adder/Subtractor Circuit

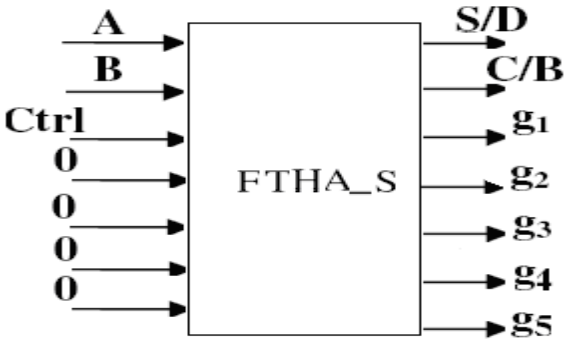


Figure 9: Half Adder/Subtractor Circuit With the 4 Constant Inputs & the 5 Garbage Outputs

B. Design of Full Adder/Subtractor Circuit (FTFA_S)

For the complete adder/subtractor conduit, the usual customary technique is followed, meaning to use two mid adder conduits. Figure 4 shows the complete adder/subtractor employing the suggested FTHA_S conduit. The expression for a complete adder is as follows:

$$\text{Sum} = A \text{ XOR } B \text{ XOR } C \qquad \text{.....(3.7)}$$

$$\text{Carry} = (A \text{ XOR } B)\ C_{in} \text{ XOR } AB \qquad \text{.....(3.8)}$$

And the expression for a complete subtractor is as follows:

$$\text{Difference} = A \text{ XOR } B \text{ XOR } B_{in} \qquad \text{.....(3.9)}$$

$$\text{Borrow} = \bar{A}B + BB_{in} + B_{in}\bar{A} \qquad \text{.....(3.10)}$$

The expressions (3.7) and (3.9) are similar whereas there is a difference in the expressions (3.8) and (3.10). Figure 5 proposes a structure that uses the recommended mid adder/subtractor. There are three contributions, namely A, B and Cin as well as the limit line 'ctrl' that controls the processing technique. When 'ctrl' is at the logic 0, the conduit functions as a complete adder and when 'ctrl' is at the logic 1, the conduit executes subtraction. The summation and diversion line is represented as the S/D and the corresponding carry and borrow by C/B. The rest of the nine steady contributions are assumed to be logic 1 and there are 11 waste outputs. The proposed fault tolerant full adder/subtractor (FTFA_S) circuit executes summation and difference by employing a solitary 'ctrl'.

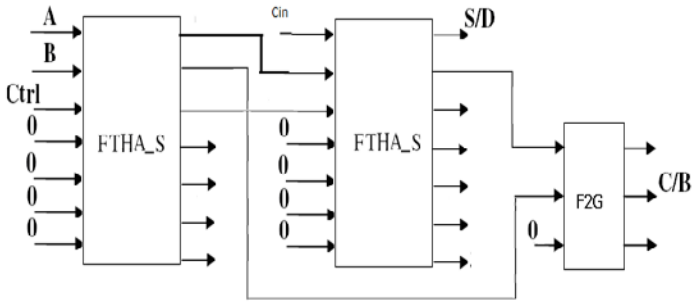


Figure 10: The Reversible Fault Tolerant Full Adder/Subtractor Circuit

4. Proposed Design

The proposed design that consists of both the adder and subtractor may operate with the help of the solitary limit line. The plan will comprise of this limit line 'Ctrl' that will select the adder or the subtractor by approving the control logic contributed data.

(i) If 'ctrl' = 0 the conduit functions as an Adder

(ii) If 'ctrl' = 1 the conduit functions as a Subtractor

This setting of adder/subtractor is improved from past plans regarding the wastage results and the constant contributions. This paper will include the plans of the reversible four bit sequential adder/subtractor, complete adder/subtractor, and mid adder/subtractor with the COG gate.

A. MIG Gate

Figure 3.6 shows the 4*4 reversible Modified Islam Gate (MIG) [10] in which the contribution vectors are A, B, C and D and the result vectors are P,Q,R and S.

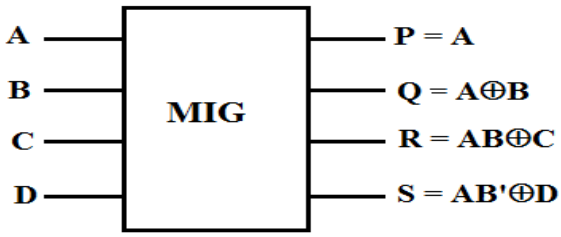


Figure 11: The MIG Gate

B. COG Gate

The 3*3 Controlled Operation Gate (COG), as shown in Figure 3.7, has three contributions A, B and C and three results P, Q and R [11].

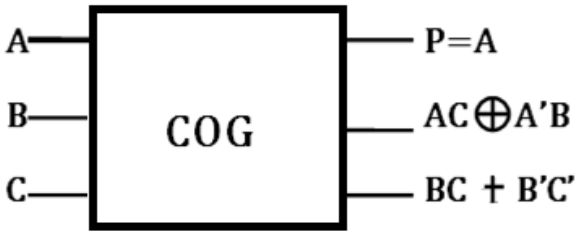


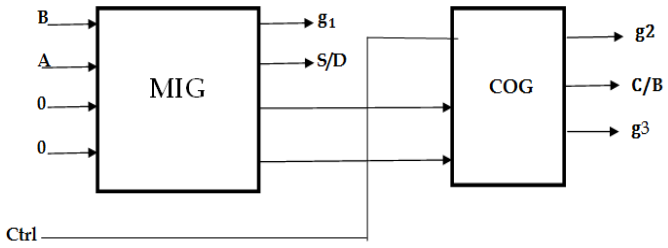
Figure 12: The COG (Controlled Operation Gate)

C. Design of the reversible Half Adder/Subtractor circuit (HA_S)

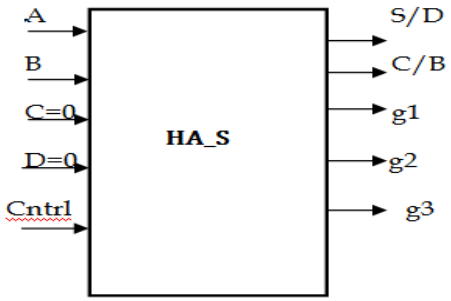
The devising of this specific structure must be feasible with the aid of MIG and COG. The limit line decides the mid adder/subtractor [12]. When 'ctrl' is at the logic 0, the conduit functions as a half adder and when 'ctrl' is at the logic 1, the conduit operates as a half subtractor. The summation and diversion line is represented as the S/D and the corresponding carry and borrow by C/B, as shown in Figure 3.8(a). The two contributions are termed constants and forced to logic 0 and the waste outputs are g1 to g3. It can be understood from Figure 3.8 (b) that a reversible mid adder/subtractor (FTHA_S) conduit compels the five contributions and similarly the five results, as per the reversible rule. The results of the proposed conduit are:

$$S/D = A \text{ XOR } B \qquad ...(3.11)$$

$$C/B = \overline{ctrl}\, AB + ctrl\, \bar{A}\, B \qquad ..(3.12)$$



(a)



(b)

Figure 13: (a) The Reversible Half Adder/Subtractor Circuit (b) The Half Adder/Subtractor circuit with the two constant-inputs & the three garbage-outputs

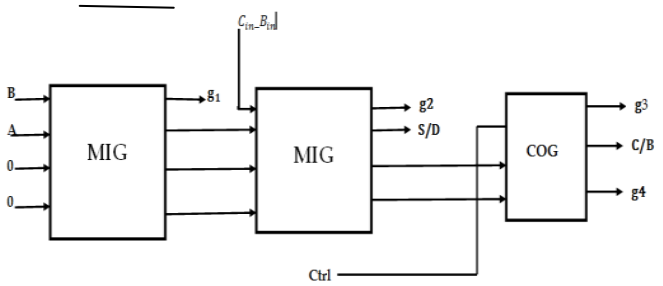
D. Design of the Reversible Full Adder/Subtractor circuit (FA_S)

The devising of this structure must be feasible with the aid of MIG and COG. The limit line decides the complete adder/subtractor. When 'ctrl' is at the logic 0, the conduit functions as a complete adder and when 'ctrl' is at the logic 1, the conduit functions as a complete subtractor. The summation and diversion are represented as the S/D and the corresponding carry and borrow by C/B as shown in Figure 3.9. The remaining of the four constant contributions are forced to be logic 0 and the waste outputs are g1 to g3. The results of the suggested circuit are:

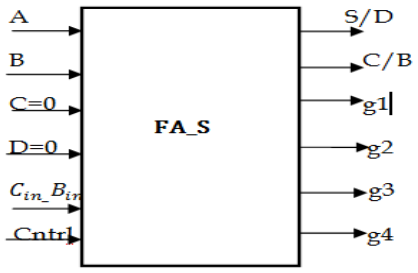
$$S = A \text{ XOR } B \text{ XOR } C_{in} \quad \ldots(3.13)$$

$$D = A \text{ XOR } B \text{ XOR } C_{in} \quad \ldots(3.14)$$

$$C/B = Cntrl\,[C_{in}\,(B \text{ XOR } A) \text{ XOR } A\,'B] + Cntrl\,'\,[C_{in}\,(B \text{ XOR } A) \text{ XOR } AB] \quad \ldots(3.15)$$



(a)



(b)

Figure 14: (A) The Reversible Full Adder/Subtractor Circuit, (B) The Half Adder/Subtractor Circuit With Four Garbage Outputs & The Two Constant Input

5. Results

Figure 4.4 displays the RTL representation for the MIG and the COG founded complete Adder/Subtractor. For the summation and subtraction of three bits, we need to use 4 bits at contributions A, B, C and Cin while the Sum/ Difference and Carry/ Borrow are the results. At the input we use the Ctrl signal to control the operations of summation and subtraction. When this signal is 0, the planned conduit will function as an adder and when it is 1 then the planned conduit will execute a subtraction.

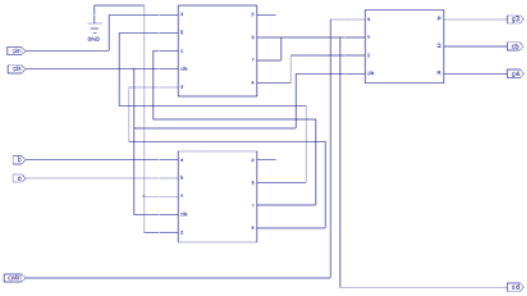


Figure 15: RTL view for MIG and COG Gate based full Adder/ Subtraction

Figure 4.5 displays the waveform for the MIG and COG founded complete adder since the control signal is 0 at the contribution. At the bits contribution we provide a, b and c as a 1,1,1 at the input end while we are getting addition equal to 1 as well as Carry equal to 1 at the output.

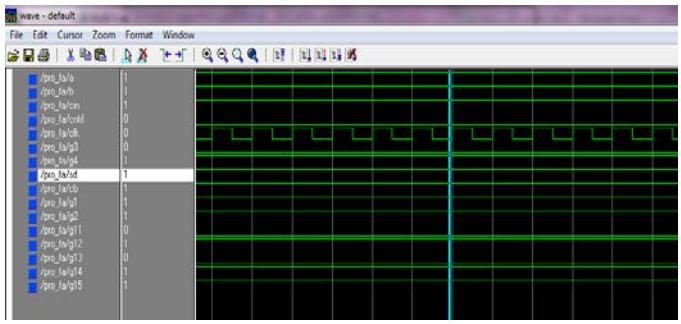


Figure 16:- MIG and COG gate based Full adder

Figure 4.6 displays the waveform for the MIG and COG founded complete subtraction. The control signal is equal to 1 at the input, therefore for contribution A, B, and Cin we are giving 1, 1, 0 while at the results we are having the Difference equal to 0 and Borrow as well equal to 0.

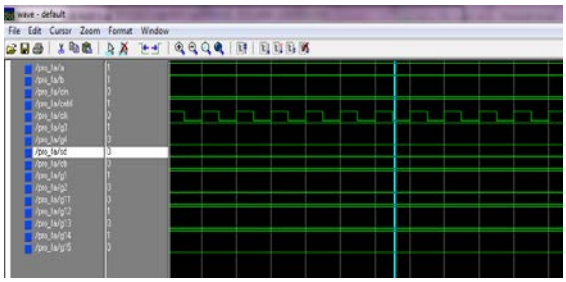


Figure 17:- MIG and COG gate based Full Subtraction

Design Name	Delay
Feynman Double Gate (F2G) and Fredkin Gate (FRG) based Fault Tolerant Full Adder / Subtraction	8.747 ns
MIG and COG Gate Based Fault Tolerant Full Adder / Subtraction	2.526 ns

Table 4: Comparison Table

Table 4.1 is the Comparison Table for the current plan and the suggested plan. We are utilizing the Fault Tolerant Full Adder that is founded on the F2G and FRG for the current plan whereas for the suggested plan we are utilizing the one founded on MIG and COG. The set-back in the first case is 8.747 ns whereas for the plan we suggested, it is 2.526 ns.

6. Conclusion And Future Scope

A. Conclusion

In this work, we showed that the Fault Tolerant Full Adder/Subtractor (FT_FAS) circuit based on the Modified Islam Gate and the Controlled Operation Gate as reversible logic gates worked with a shorter set-back so as to improve the performance aspect of the rapid adder and subtractor. It is clear from the Results section that the set-back is reduced as much as 61% with the MIG and COG sort of reversible logic gates. We have demonstrated the feasibility of using the equivalence conserving method to plan these reversible logic conduits. The technique paves the way to integrate error leniency in the reversible conduits with no surplus endeavors of designing and with unassuming equipment available, this is an aim that has so far been evidenced as challenging.

7. References

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